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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/550,405	04/14/2000	Eiji IO	APM-01301	8514

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EXAMINER
NADAV, ORI

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/07/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/550,405	IO, EIJI	
	Examiner	Art Unit	
	ori nadav	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 20-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 20-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *14* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to because of the following informalities: Claim 6 recites low resistive wiring layers being located outwardly beyond a peripheral edge of a sidewall offset. Dependent claim 22 recites forming only one sidewall offset. It is unclear how a wiring layer can be located beyond a peripheral edge of a sidewall offset which does not exist. Appropriate correction is required.

2. Claim 22 is objected to because of the following informalities: Claim 22 recites forming a sidewall offset in the source and drain regions. It is unclear how a sidewall offset can be formed in the source and drain regions since the sidewall offset is located over the source and drain regions above the gate oxide. Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-11 and 20-23 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is no support for at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction, as recited in claims 1 and 6. In fact, figures 3 and 4 depict the source and drain region layers 65, 66 extending towards the gate electrode beyond an edge of the sidewall offset by an amount smaller than a depth of the source and drain region layers in a vertical direction

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 5 and 20, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez (5,439,835).

Gonzalez teaches in figure 9 a semiconductor device comprising a memory cell formed on a semiconductor substrate 12, an insulating layer 13 defining device regions, a gate region 16, source and drain regions 23 (figure 2) around the gate electrode, at least one sidewall 41 (figure 4) covering the gate electrode and having a sidewall offset extending outwardly of the gate electrode along a surface of the substrate above only one of the source and drain regions and along a surface of a gate oxide, low resistive wiring layers 92, 51 (figure 5) formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset, at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset.

Gonzalez does not explicitly state that at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction. Figure 9 depicts at least one of the source and drain region layers (located adjacent to FOX region 13) extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an

amount greater than a depth of the source and drain region layers in a vertical direction in Gonzalez's device, in order to improve the device characteristics by adjusting the threshold voltage of the device.

7. Claims 3-4, 6, 9-11 and 22, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Cheng et al. (5,545,575).

Gonzalez teaches substantially the entire claimed structure, as applied to claim 1 above, except second diffusion layers of lower impurity concentration than that of the source and drain regions formed below the source and drain regions.

Cheng et al. teach in figure 7 second diffusion layers 43, 44 of lower impurity concentration than that of the source and drain regions (column 4, lines 24-26 and column 6, lines 2-4) formed below the source and drain regions.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form lower impurity concentration second diffusion layers below the source and drain regions in Gonzalez's device, in order to improve the device characteristics.

Regarding claims 6, 11 and 22, Cheng et al. teach in figure 7 silicide wiring layers 64 formed at surfaces and in the source and drain layers located outwardly beyond a

peripheral edge of the sidewall offset. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form silicide wiring layers at surfaces and in the source and drain layers located outwardly beyond a peripheral edge of the sidewall offset in Gonzalez's device in order to reduce the contact resistance of the device.

8. Claim 7, insofar as in compliance with 35 U.S.C. 112, is rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez and Cheng et al., as applied to claim 6 above, and further in view of Kunishima et al. (5,316,977).
Gonzalez and Cheng et al. teach substantially the entire claimed structure, as applied to claim 1 above, except a silicide layer comprising titanium silicide.
Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.
It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Gonzalez and Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice is taken.

9. Claims 1-4, 6, 8-10, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al.

Cheng et al. teach in figure 15 a semiconductor device comprising a semiconductor substrate 11, an insulating layer 19 defining device regions, a gate region 28, source and drain regions 57, 58 around the gate electrode, a sidewall 66 covering the gate electrode and having a sidewall offset extending outwardly of the gate electrode along a surface of the substrate in both regions above the source and drain regions and along a surface of a gate oxide, silicide wiring layers 64 formed at surfaces of the source and drain layers being located outwardly beyond a peripheral edge of the sidewall offset, at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset, and second diffusion layers 43, 44 of lower impurity concentration than that of the source and drain regions (column 4, lines 24-26 and column 6, lines 2-4) formed below and surrounding the source and drain layers.

Although Cheng et al. do not explicitly state that a sidewall offset extends outwardly of the gate electrode along a surface of a gate oxide, figure 15 depicts a sloped sidewall offset being located outwardly of the vertical sidewall and along a surface of the gate oxide. Therefore, Cheng et al. teach a sidewall offset extends outwardly of the gate electrode along a surface of a gate oxide.

Cheng et al. do not explicitly state that at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical

direction. Figure 15 depicts at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction in Cheng et al.'s device, in order to improve the device characteristics by adjusting the threshold voltage of the device.

Regarding claims 21 and 23, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

10. Claims 5, 7, 11, 21 and 23, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheng et al., as applied to claims 1 and 6 above, and further in view of Kunishima et al.

Cheng et al. teach substantially the entire claimed structure, as applied to claims 1 and 6 above, except a silicide layer comprising titanium silicide.

Kunishima et al. teach in figure 5C a silicide layer 21 comprising titanium silicide.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a titanium silicide in Cheng et al.'s device, because titanium silicide is a conventional silicide material, of which official notice may be taken.

Regarding claims 5 and 11, Kunishima et al. teach using the semiconductor device as a CMOS device, and it is well known in the art that CMOS devices are used as memory devices.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use Cheng et al.'s device as a memory device, because the intended use of a device depends on the requirements of the application in hand.

Note that a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. See *In re Casey*, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 136 USPQ 458, 459 (CCPA 1963).

Regarding claims 21 and 23, Kunishima et al. teach in figure 5C a sidewall entirely covering the gate electrode. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to cover entirely the gate electrode of Cheng et al.'s device with the sidewall in order to provide better protection for the gate in an application which does not require external connection to the gate.

Response to Arguments

11. Applicant argues that Gonzalez does not teach in figure 9 at least one of the source and drain region layers extending towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction, because diffusions 23 and 71 are aligned to sidewalls 21 and 41, respectively.

It appears that applicant refers to source and drain regions connected to bit line 92. However, the rejection recites source and drain regions 23 located adjacent to FOX region 13. These source and drain region layers 23 extend towards the gate electrode beyond an edge of the sidewall offset by an amount greater than a depth of the source and drain region layers in a vertical direction, as claimed.

12. Applicant traverses on pages 8 and 9 the rejection of claims 3-4, 6, 9-11 and 22 under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Cheng et al., because Cheng et al. do not teach a sidewall offset extending along a surface of the gate oxide.

Claims 3-4, 6, 9-11 and 22, insofar as in compliance with 35 U.S.C. 112, are rejected under 35 U.S.C. 103(a) as being unpatentable over Gonzalez in view of Cheng et al. Gonzalez teaches substantially the entire claimed structure, as applied to claim 1 above, wherein Cheng et al. is cited to teach second diffusion layers of lower impurity concentration than that of the source and drain regions formed below the source and drain regions.

13. In response to applicant's argument on page 11 that Cheng et al. fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., a sidewall limiting the location of a part of the structure) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 3 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Tom Thomas

Ori Nadav

February 4, 2002

TOM THOMAS
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